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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,694	03/05/2002	Bruce E. Lavigne	100202225-1	7434

7590 01/29/2007

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EXAMINER	
ABELSON, RONALD B	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/091,694	LAVIGNE ET AL.	
	Examiner	Art Unit	
	Ronald Abelson	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10,12,15-19 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10,12,15-19 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/5/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 4, 5, 19, and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCloghrie in view of Genrich (US 5,596,609).

Regarding claims 1, 19, and 23, McCloghrie teaches a processor (fig. 1 box 120, col. 3 lines 31-34).

McCloghrie teaches an input interface for receiving a plurality of packets coupled to the processor (fig. 1 element 111, col. 3 lines 31-34), the input interface comprising at least one input port wherein at least one said input port is configured to sample at least one input packet and transmit a sampled input packet to the processor (fig. 1 box 111, sampling of packets occurs at input interfaces 111, forwards sampled packets to another portion of traffic management element 120, col. 3 lines 42-52), wherein at least one said input port comprises a countdown register, wherein said input port is configured to sample a packet according to said countdown register (fig. 1 box 111, sampling of packets occurs at the input interfaces, col. 3 lines 42-45, sample one out of every N packets, col. 4 lines 41-43).

McCloghrie teaches an output interface for transmitting a plurality of packets coupled to the processor (fig. 1 element

112, col. 3 lines 31-34), the output interface comprising at least one output port wherein at least one said output port is configured to sample at least one output packet and transmit a sampled output packet to the processor (fig. 1 box 112, sampling of packets occurs at output interfaces 112, forwards sampled packets to another portion of traffic management element 120, col. 3 lines 42-52), wherein said input interface and said output interface feed into said processor (traffic management element 120 is coupled to substantially all input interfaces and substantially all output interfaces, col. 3 lines 31-41), wherein at least one said output port comprises a countdown register, wherein said output port is configured to sample a packet according to said countdown register (fig. 1 box 112, sampling of packets occurs at the output interfaces, col. 3 lines 42-45, sample one out of every N packets, col. 4 lines 41-43).

McCloghrie teaches a switching fabric coupled to the input interface and the output interface, the switching fabric configured to transmit a packet between the input interface and output interface (fig. 1 box 110, col. 3 lines 22-29).

Regarding claim 23, in addition to the limitations previously addressed, a computer-readable memory coupled to said

input interface and said output interface (fig. 1 box 130, col. 4 lines 1-5) and a microcontroller coupled to said input interface and said output interface, said microcontroller for executing a method of sampling a packet (fig. 2 Sampling CTRLR, col. 4 lines 19-21).

Although McCloghrie teaches a processor (fig. 1 box 120) that performs sampling, the reference does not explicitly the processor is integrated with the network device (fig. 1 box 110).

Genrich teaches a processor integrated within the network device / integrated circuit capable of performing the sampling functions listed above (integrated circuit, sampling rate, col. 3 lines 39-42).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of McCloghrie by incorporating the sampling functions (fig. 1 box 120) on a single integrated circuit within the router/switch (fig. 1 box 110). This modification can be performed according to the teachings of Genrich. This modification would benefit the system by allowing for all the functions to be performed on a single, reliable, inexpensive device.

Regarding claims 4 and 22, the processor (fig. 1 box 120, fig. 2 box 120) transmits said sampled input packet and said sampled output packet to a central control station (fig. 2 see transmission of packet from box 250 to 260, col. 5 lines 62-65) over a network. The Examiner corresponds applicant's central control station with the Type Detector and Frequency Measure (fig. 2 box 260, 270) of the reference and the applicant's network with the connection from box 250 to 260 in the reference.

Regarding claim 5, the central control station comprises a statistical monitoring station (fig. 2 box 270, col. 6 lines 8-13).

Regarding claims 24 and 25, the microcontroller transmitting said sampled incoming/outgoing packet to a statistical monitoring station (fig. 2 box 270) over a network (see the connection from box 250 to 260).

3. Claims 10, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCloghrie in view of Genrich (US 5,596,609).

Regarding claim 10, McCloghrie teaches for receiving a plurality of packets at an input network circuit, said input network circuit comprising at least one input port (fig. 1 element 111, col. 3 lines 31-34).

McCloghrie teaches sampling at least one input packet, wherein said sampling comprises using a countdown circuit (fig. 1 box 111, sampling of packets occurs at input interfaces 111, sample one out of every N packets, col. 4 lines 41-43)

McCloghrie teaches transmitting at least one sampled input packet to a processor (forwards sampled packets to another portion of traffic management element 120, col. 3 lines 42-52).

McCloghrie teaches transmitting at least one packet from said network circuit to an output network circuit (fig. 1: see output of box 120 to box 130) over a switching fabric (fig. 1 box 110), said output network circuit comprising at least one output port.

McCloghrie teaches sampling at least at least one output packet at said output port (fig. 1 see connection from output port 112 to box 120).

McCloghrie teaches transmitting at least one packet from said input network circuit to an output network circuit of said network device over a switching fabric of said network device, said output network circuit comprising at least one output port (fig. 1 see connection from port 111 to port 112 through router/switch box 110) wherein said input network circuit and said output network circuit feed into said processor (traffic management element 120 is coupled to substantially all input interfaces and substantially all output interfaces, col. 3 lines 31-41).

Although McCloghrie teaches a processor (fig. 1 box 120) that performs sampling, the reference does not explicitly the processor is integrated with the network device (fig. 1 box 110).

Genrich teaches a network device / integrated circuit capable of performing the sampling functions listed above (integrated circuit, sampling rate, col. 3 lines 39-42).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of McCloghrie by incorporating the sampling functions (fig. 1 box 120) on a single integrated circuit within the router/switch (fig. 1 box 110). This modification can be performed according to the

teachings of Genrich. This modification would benefit the system by allowing for all the functions to be performed on a single, reliable, inexpensive device.

Regarding claim 15, the processor (fig. 1 box 120, fig. 2 box 120) transmitting said sampled input packet (fig. 1,2 box 120, col. 5 lines 62-65) to a statistical monitoring station (fig. 2 box 270, col. 6 lines 8-13) over a network (see connection from box 250 to 260).

Regarding claim 16, the processor (fig. 1 box 120, fig. 2 box 120) transmitting said sampled output packet (fig. 1,2 box 120, col. 5 lines 62-65) to a statistical monitoring station (fig. 2 box 270, col. 6 lines 8-13) over a network (see connection from box 250 to 260).

4. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie and Genrich as applied to claim 1 above, and further in view of Dean (US 6,442,585).

Regarding claims 8 and 9, although McCloghrie teaches a countdown register, the reference is silent on a random number countdown register.

Dean teaches a random number countdown register (fig. 2 box 265, countdown register, random sampling, col. 7 lines 31-37).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by replacing the countdown registers at the input and output ports with a random number countdown register as suggested by Dean. This modification would benefit the system by providing for improved statistical sampling.

5. Claim 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie and Genrich as applied to claim 10 above, and further in view of Dean (US 6,442,585).

Regarding claim 12, although the combination of McCloghrie and Genrich teaches a countdown register, the reference is silent on a random number countdown register.

Dean teaches a random number countdown register (fig. 2 box 265, countdown register, random sampling, col. 7 lines 31-37).

Therefore it would have been obvious to one of ordinary

skill in the art, to modify the system of the combination of McCloghrie and Genrich by replacing the countdown registers at the input and output ports with a random number countdown register as suggested by Dean. This modification would benefit the system by providing for improved statistical sampling.

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie and Genrich as applied to claim 1 above, and further in view of Chen (US 6,658,006).

Regarding claim 6, the combination is silent on the sampled input packet comprises an identification of the input port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of an incoming packet to identify the input port (col. 1 lines 48-51).

Regarding claim 7, the combination is silent on the sampled output packet comprises an identification of the output port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of a packet to identify the output port (col. 1 lines 51-55).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination by incorporating within the input and output ports logic to modify the header bits to identify the respective input/output ports. This modification can be performed according to the teachings of Chen. This information could be useful in load balancing.

7. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie and Genrich as applied to claim 10 above, and further in view of Chen (US 6,658,006).

Regarding claim 17, the combination of McCloghrie and Genrich is silent on the sampled input packet comprises an identification of the input port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of an incoming packet to identify the input port (col. 1 lines 48-51).

Regarding claim 18, the combination of McCloghrie and Genrich is silent on the sampled output packet comprises an identification of the output port that sampled the sampled input packet.

Chen teaches a method for modifying the header bits of a packet to identify the output port (col. 1 lines 51-55).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of McCloghrie and Genrich by incorporating within the input and output ports logic to modify the header bits to identify the respective input/output ports. This modification can be performed according to the teachings of Chen. This information could be useful in load balancing.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McCloghrie and Genrich as applied to claim 10 above, and further in view of Dean (US 6,442,585).

Although McCloghrie teaches a countdown register, the combination is silent on a random number countdown register.

Dean teaches a random number countdown register (fig. 2 box 265, countdown register, random sampling, col. 7 lines 31-37).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of

McCloghrie and Genrich by replacing the countdown registers at the input and output ports with a random number countdown register as suggested by Dean. This modification would benefit the system by providing for improved statistical sampling.

Response to Arguments

9. Applicant's arguments with respect to independent claims 1, 19, and 23 have been considered but are moot in view of the new ground(s) of rejection. Regarding the 102(e) rejection (applicant: pg. 8) this is an obvious careless error. The rejection should have been a 103. The Examiner has corrected the error.

Regarding applicant's response to dependent claims 4, 5, 24, and 25 (applicant: pg. 11 1st paragraph), the applicant states that the limitations are not met, but does not state why. The Examiner maintains the rejections to these claims.

The applicant contends that Genrich does not disclose an integrated circuit capable of performing sampling functions (applicant: pg. 14 1st paragraph). However, Ginrich teaches an integrated circuit having a defined sampling rate (col. 3 lines

39-42). Regarding applicant's statement that Genrich does not provide any suggestion or motivation to modify (applicant: pg. 14 1st paragraph) and neither McCloghrie nor Genrich include a suggestion that benefits are provided (applicant: pg. 15 1st paragraph):

The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art at the time the invention was made. See In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Regarding applicant's assertion that the Examiner is relying on impressible hindsight (applicant: pg. 14 last paragraph), the benefits of integrated circuits are well known. Throughout the remainder of his remarks, the applicant reiterates the impressible hindsight argument. The Examiner maintains that the benefits of integrates circuits were well known at the time of the invention.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Ronald Abelson whose telephone number is (571) 272-3165. The Examiner can normally be reached on M-F.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ronald Abelson
Examiner
Art Unit 2616